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FPGA Implementation For Improve in Orthogonal Code Convolution

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***Abstract* – As the data is communicated and stored through a communication channel such as cable or wire the parameters like noise or crosstalk can impact this data, so to correct these types of errors the techniques are orthogonal codes. An n-bit orthogonal code has n/2 1s and n/2 0s. In a previous work these properties have been exploited to detect and correct errors. In this paper we are representing the new method to improve error detection .The result will improve error detection capacity by 40% of the orthogonal codes.**

***Keywords* — FPGA, Orthogonal Code Convolution.**

I. INTRODUCTION

As the data is communicated and stored through a communication channel such as cable or wire the parameters like noise or crosstalk can impact this data, so to correct this types of errors the techniques are orthogonal codes However, the existing techniques are not able to achieve high efficiency and to meet bandwidth requirements, especially with the increase in the quantity of data transmitted. Orthogonal Code is one of the codes that can detect errors and correct corrupted data.

II. ORTHOGONAL CODES

Orthogonal codes are binary valued and they have equal number of 1's and 0's. An n-bit orthogonal code has n/2 1's and n/2 0's; i.e., there are n/2 positions where 1's and 0's differ. Therefore, all orthogonal codes will generate zero parity bits. Since there is an equal number of 1's and 0's, each orthogonal code will generate a zero parity bit. Therefore, each antipodal code will also generate a zero parity bit. A notable distinction in this method is that the transmitter does not have to send the parity bit since the parity bit is known to be always zero. Therefore, if there is a transmission error, the receiver will be able to detect it by generating a parity bit at the receiving end.

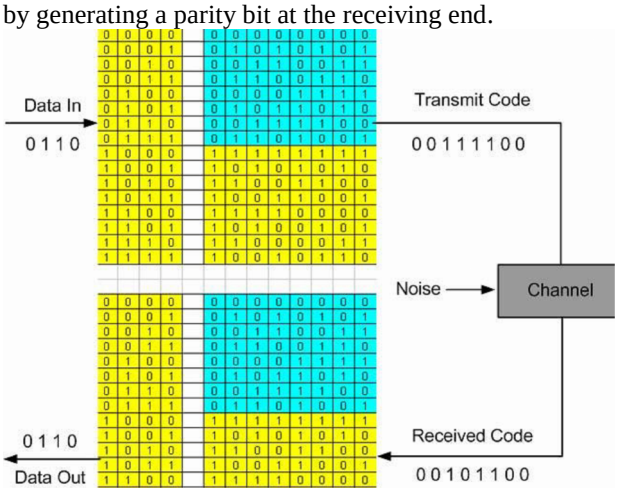

Fig.1. Representation of encoding & decoding

This offers a decision process, where the, incoming impaired orthogonal code is examined for correlation with the neighboring codes for a possible match.

The acceptance criterion for a valid code is that an n-bit comparison must yield a good auto-correlation value; otherwise, a false detection will occur. This is governed by the following correlation process, where a pair of n-bit codes x_1, x_2... xn and y_1, y_2 … yn is compared to yield.

Therefore the equations comes are

$$D = N/4 \quad \text{…….. (1)}$$

And the other equation becomes as

$$R(x, y) = x1y1 < n/4 - 1 \quad \text{…… (2)}$$

Where R(x, y) is the auto correlation function, n is the code length, d_{th} is the threshold defined in (1). Since the threshold (d_{th}) is in between two valid codes, an additional 1-bit offset is added to (2) for reliable detection. The average number of errors that can be corrected by means of this process can be estimated by combining (1) and (2), yielding.

Therefore the equation three becomes

$$T = n\text{-}R(x,y) = n/4\text{-}1 \quad \text{……} \quad (3)$$

In (3), t is the number of errors that can be corrected by means of an n-bit orthogonal code. For example, a single error-correcting orthogonal code can be constructed by means of an 8-bit orthogonal code (n = 8).

III. FPGA IMPLEMENTATION AND METHODS

3.1 Design Methodology

Since there is an equal number of 1's and 0's, each orthogonal code will generate a zero parity bit. If the data has been corrupted during the transmission the receiver can detect errors by generating the parity bit for the received code and if it is not zero then the data is corrupted. However the parity bit doesn't change for an even number of errors, hence the receiver can only detect errors 2_n /2 combinations of the received code. Therefore detection percentage is 50% . Our approach is not to use the parity generation method to detect the errors, but a simple technique based on the comparison between the received code and all the orthogonal code combinations stored in a look up table. The technique which involves the transmitter and receiver is describe as follows.

3.2 Transmitter

The transmitter includes two blocks: an encoder and a shift register. The encoder encodes a k-bit data set to $n=2_{k-1}$ bits of the orthogonal code and the shift register transforms this code to a serial data in order to be transmitted.

For example, 4-bit data is encoded to 8-bit (2_3) orthogonal code. The generated orthogonal code is then transmitted serially using a shift register with the rising edge of the clock.

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3.3 Receiver

The received code is processed through the sequential steps, The incoming serial bits are converted into n-bit parallel codes. The received code is compared with all the codes in the lookup table for error detection. This is done by counting the number of ones in the signal resulting from 'XOR' operation between the received code and each combination of the orthogonal codes in the lookup table. A counter is used to count the number of ones in the resulting n-bit signal and also searches for the minimum count. However a value rather than zero shows an error in the received code. The orthogonal code in the lookup table which is associated with the minimum count is the closest match for the corrupted received code. The receiver is able to correct up to (n/4)-1 bits in the received impaired code associated with one combination of Orthogonal code.

IV. IMPLEMENTATION AND RESULTS

An hardware board Xillinx software have been used for code testing. The simulation has been performed using ModelSim XE software. The simulation results were verified for most of the combinations of 8-bit and some of the 16-bit orthogonal code. The software simulation results along with the clock cycles are explained for the transmitter and receiver.

4.1 Transmitter

The transmitter simulation corresponding to the input data value "0110" labeled as 'data'. This data has been encoded to the associated orthogonal code "00111100" labeled 'ortho'. The signal 'EN' is used to enable the transmission of the serial bits 'txcode' of the orthogonal code with every rising edge of the clock.

4.2 Receiver

Upon reception, the incoming serial data is converted into 8-bit parallel code 'rxcode. Counter is used to count the number of 1's after XOR operation between the received code and all combinations of orthogonal code in the lookup table. 'Count' gives the minimum count of ones among them. The orthogonal code 'ortho' associated with the minimum count is the closest match for the received code, which is then decoded to the final data given by signal 'data'. Three different cases result from this simulation. In the first case, the received code has a match in the lookup table, the received code is rxcode = "00111100", count='0' and hence the received code is not corrupted. The code is then decoded to the corresponding final data "0110".

In the second case, the received code has no match in the lookup table. The received code is rxcode="00110100", the value of minimum count is '1', which reveals an error. The corresponding orthogonal code is ortho= "00111100" which is the closest match for the received code given by the minimum count, and the decoded final data is "0110". In this case the single bit error is detected and corrected by the receiver.

In the third case, there is more than one possibility of closest match in the lookup table. The received code is rxcode= "00110000". The value of minimum count is associated with more than one orthogonal code and thus it is not possible to determine the closest match in the lookup table for the received code. Then the signal labeled 'REQ' goes high, which is a request for a retransmission.

4.3 Results

The results of the simulation show that for a k-bit data, the corresponding n-bit orthogonal code is able to detect any faulty combination other than the combinations of orthogonal code in the lookup table. The numbers of these combinations are 2_k. Hence the percentage of detection is given by $(2_n-2_k)/2_n$ %. Similarly, the system is able to correct up to (n/4)-1 bit error and the number of clock cycles required to process the received code are (2n+2). For example when a 4-bit data is encoded in to 8- bit orthogonal code; it has $2_4 = 16$ combinations of orthogonal code. Therefore, out of 256 possible combinations of 8-bit received code the receiver will not able to detect error in those codes which are one of the combinations of orthogonal code. Hence the detection percentage for 8-bit orthogonal code is given by $(2_8 - 2_4)/2_8 = 93.57\%$ and also able to correct single bit error. Similarly, the percentage of detection for 16-bit orthogonal code is 99.95%.The simulation of transmitter is inputed the data "0110"and it is encoded in orthogonal code"00111100" and it checks the priority and thus provides the results.

V. CONCLUSION

The result of Orthogonal Code implementation is improves from 50% to 95 %. Future work includes improvement of correction of errors more efficiently and it also improves the accuracy of the operation of functioning circuit improves the performance due to Orthogonal Code implementation.

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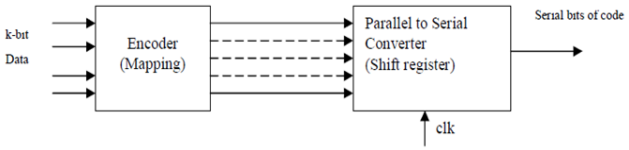

Fig.2. Block diagram of the transmitter.

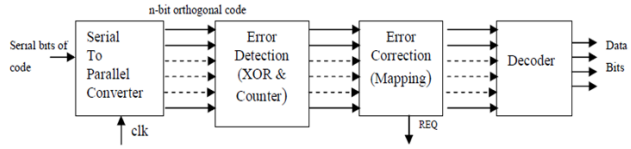

Fig.3. Block diagram of the receiver.

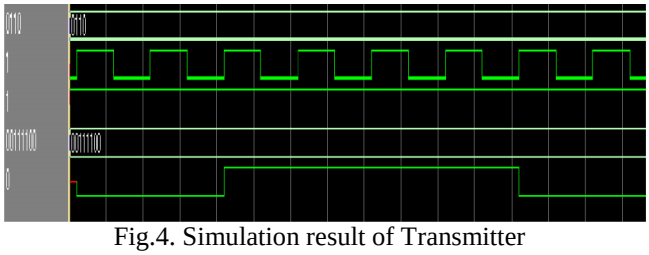

Fig.4. Simulation result of Transmitter

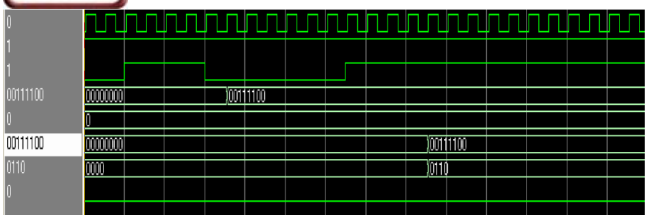

Fig.5. Case 1 simulation

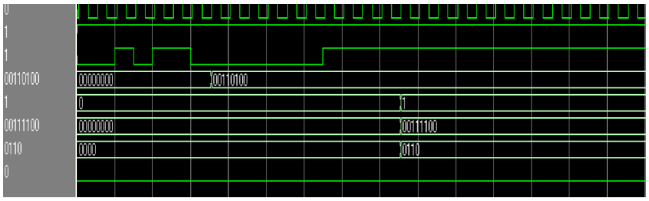

Fig.6. Case 2 simulation

REFERENCES

[1] Baicheva, T., S. Dodunekov, and P. Kazakov, "Undetected error probability performance of cyclic redundancy- check codes of 16-bit redundancy," *IEEE Proc. Comms.*, Vol. 147, No. 5, Oct. 2000, pp. 253-256.

[2] A. Hokanin, H. Delic, S. Sarin, "Two dimensional CRC for efficient transmission of ATM Cells over CDMA," *IEEE Communications* Letters, Vol. 4, No. 4, April 2000.

[3] Stylianakis V ,Toptchiyski S, "A Reed-Solomon coding/decoding structure for an ADS modem", Electronics, *Circuits and Systems*, 1999. Proceedings of ICECS apos ; 99. The 6th *IEEE International Conference*, Volume 1, Issue, 1999, pp. 473 – 476.

[4] S. Faruque, "Broadband Communications Based on Code Division Parallel Access (CDPA)", *The International Engineering Consortium (IEC)*, Annual Review of Communications, Vol. 57, ISBN: 1-931695-28-8, Nov. 2004.

[5] Saleh Faruque , "Error Control Coding Based on Orthogonal Codes", *Wireless Proceedings*, Vol. 2, pp. 608-615, 2004.

[6] S. Faruque, A.Dhirde ,N.Kaabouch "Forward error control coding based on orthogonal code and its implementation using FPGA", *7th IASTED International Conference*, Montreal, Quebec, Canada, May 30 – June 1, 2007, Unpublished.

[7] B. Sklar, *Digital Communications Fundamentals and Applications*, Prentice Hall, 1998.

[8] Qualcomm, *The CDMA Network Engineering Handbook*, Vol. I, Concepts in CDMA, 1993.

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